together with said dummy interconnections to a stable potential line which is included in said interconnections and which holds a constant potential with respect to a potential carried on a lower-potential power-supply line or a higher-potential power-supply line.

23. The semiconductor device according to claim 11, comprising:

a conductive dummy plug selectively buried in said interlayer insulating films to connect said dummy interconnections between said two or more layers and connected together with said dummy interconnections to a stable potential line which is included in said interconnections and which holds a constant potential with respect to a potential carried on a lower-potential power-supply line or a higher-potential power-supply line.

REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 1, 7-15 and 21-23 are now present in this application, Claims 2-6 and 16-20 being canceled and Claims 21-23 being added by way of the present amendment. Each of Claims 21-23 are supported by the specification and thus no question of introduction of new matter is raised. Claims 1 and 9 stand rejected under 35 USC § 102 over JP 4-179126 ('126). Under 35 USC § 103(a) Claims 1, 7-9 and 13-15 stand rejected over JP 10-199882 ('882) in view of either US 5,441,915 (Lee) or US 5,729,047 (Ma). Claims 10-12 were found to be allowable if rewritten into independent form. Claims 2-6 and 16-20 have been withdrawn from consideration as directed to a non-elected invention.

The Applicants greatly appreciate the finding of Claims 10-12 to be allowable if rewritten in independent form. Claims 10 and 11 have been amended to include elements from claim 1 and are now both independent. New Claims 21 and 22 correspond to original Claims 10 and 11. It is respectfully submitted that Claims 10-12 and new Claims 21 and 22 are in condition for allowance.

Regarding the objection of the title, a new title has been added that is clearly indicative of the invention to which the claims are directed.

In response to the objection to the drawings, Figs. 27-36 are being labeled "Prior Art" as requested in the outstanding Office Action. A separate letter requesting approval of these changes is being submitted to the draftsperson.

Claims 1 and 9 stand rejected under 35 U.S.C. § 102(b) as anticipated by '126. This rejection is respectfully traversed.

Applicants note the drawings of '126 fails to disclose other wirings located on the formation layer of metal layer for shielding 16 that corresponds to dummy interconnections of the present application.

Therefore, the metal layers for shielding 16 of '126 do not correspond to "conductive dummy interconnections provided in the same layers as said interconnection," as recited in Claim 1.

Further, as described in the specification at page 26, lines 2-6, the dummy interconnections are provided for the purpose of reducing a step height while the dummy interconnections do not directly contribute to the circuit operation. Thus, considering this purpose, the dummy interconnections must be provided in the same layer as other interconnections (interconnections which contribute directly to the circuit operation). Therefore, '126 does not teach or disclose dummy interconnections provided in the same layers as the interconnections.

Accordingly, it is respectfully submitted independent Claim 1 and Claim 9, which depends on Claim 1, are allowable.

Claims 1, 7-9 and 13-15 were rejected under 35 U.S.C. § 103(a) as unpatentable over '882 in view of either Lee or Ma. This rejection is respectfully traversed.

The outstanding Office Action states at page 4, item 7, that '882 does not disclose the dummy interconnections and dummy plug being connected to a stable potential.

Lee discloses in Figure 12 dummy lines 44 connected to a ground potential, but the disclosure shows the possibility of a single layer dummy connection being connected to a ground potential, and is not paramount to disclosing the structure of the present invention wherein dummy plugs are formed in a plurality of layers.

Further, a signal line 60 is shown in Lee being set to the ground potential, and the signal line 60 does not suggest at all "a stable potential line which is included in said interconnections and which holds a constant potential with respect to a potential carried on a lower-potential power-supply line or a higher-potential power-supply line," as recited in Claim 1. Therefore, Lee does not teach or disclose the arrangement of a dummy plug formed between two or more layers where connections are formed and connected to the above-mentioned stable potential line.

Ma discloses in Figure 3 a signal separation structure in which a signal line 90 is provided in four sides surrounded by conductive layers 102, 104, 106, and 108, connected to a ground potential. Accordingly, Ma does not disclose anything further than what it has already been disclosed by Lee in relation to the present invention.

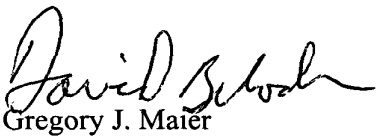
Therefore, even applying the disclosure of Lee or Ma to the teachings of '882, it is not possible to reach the structure of "a...dummy plug...connected together with said dummy interconnections to a stable potential line which is included in said interconnections and which holds a constant potential with respect to a potential carried on a lower-potential power-supply line or a higher-potential power-supply line," as recited in Claim 1.

Accordingly, it is respectfully submitted independent Claim 1 and each of the claims depending therefrom are allowable.

It is respectfully submitted that the present application is in condition for allowance and a favorable decision to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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Serial No: 09/612,298
Amendment Filed on: April 3, 2002

IN THE TITLE

Page 1, line 2, delete in its entirety and substitute therefor:

SEMICONDUCTOR DEVICE HAVING MULTILAYER INTERCONNECTION STRUCTURE

IN THE CLAIMS

Please amend the claims as follows:

10. (Amended) A [The] semiconductor device [according to claim 1,] comprising:

a semiconductor substrate having a main surface along which a semiconductor element is formed;

interlayer insulating films formed on said main surface;

conductive interconnections provided in a plurality of layers separated by said interlayer insulating films; and

conductive dummy interconnections provided in the same layers as said interconnections in two or more layers included in said plurality of layers;

wherein at least one of said dummy interconnections has repetitive protrusions and recesses along its elongate direction in a section taken along said main surface.

11. (Amended) A [The] semiconductor device [according to claim 1,] comprising:

a semiconductor substrate having a main surface along which a semiconductor element is formed;

interlayer insulating films formed on said main surface;

conductive interconnections provided in a plurality of layers separated by said interlayer insulating films; and

conductive dummy interconnections provided in the same layers as said interconnections in two or more layers included in said plurality of layers,

wherein at least one of said dummy interconnections has repetitive protrusions and recesses along its elongate direction in a section taken along a plane perpendicular to said main surface.

Claims 2-6 and 16-20 (canceled).

Claims 21-23 (New).

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